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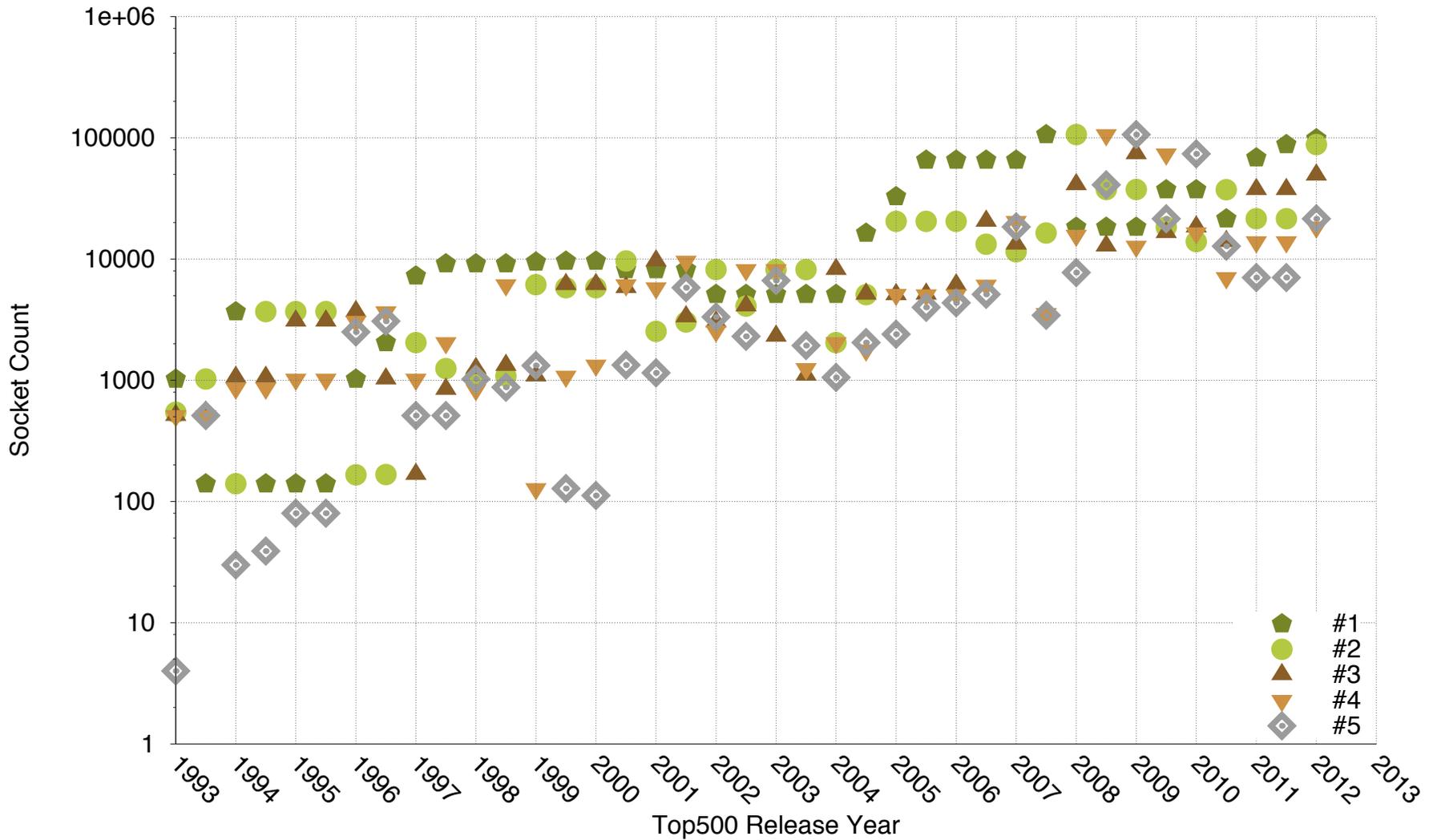
Evaluating Operating System Vulnerability to Memory Errors

Kurt B. Ferreira, Kevin Pedretti, Patrick Bridges,
Ron Brightwell, David Fiala, and Frank Mueller

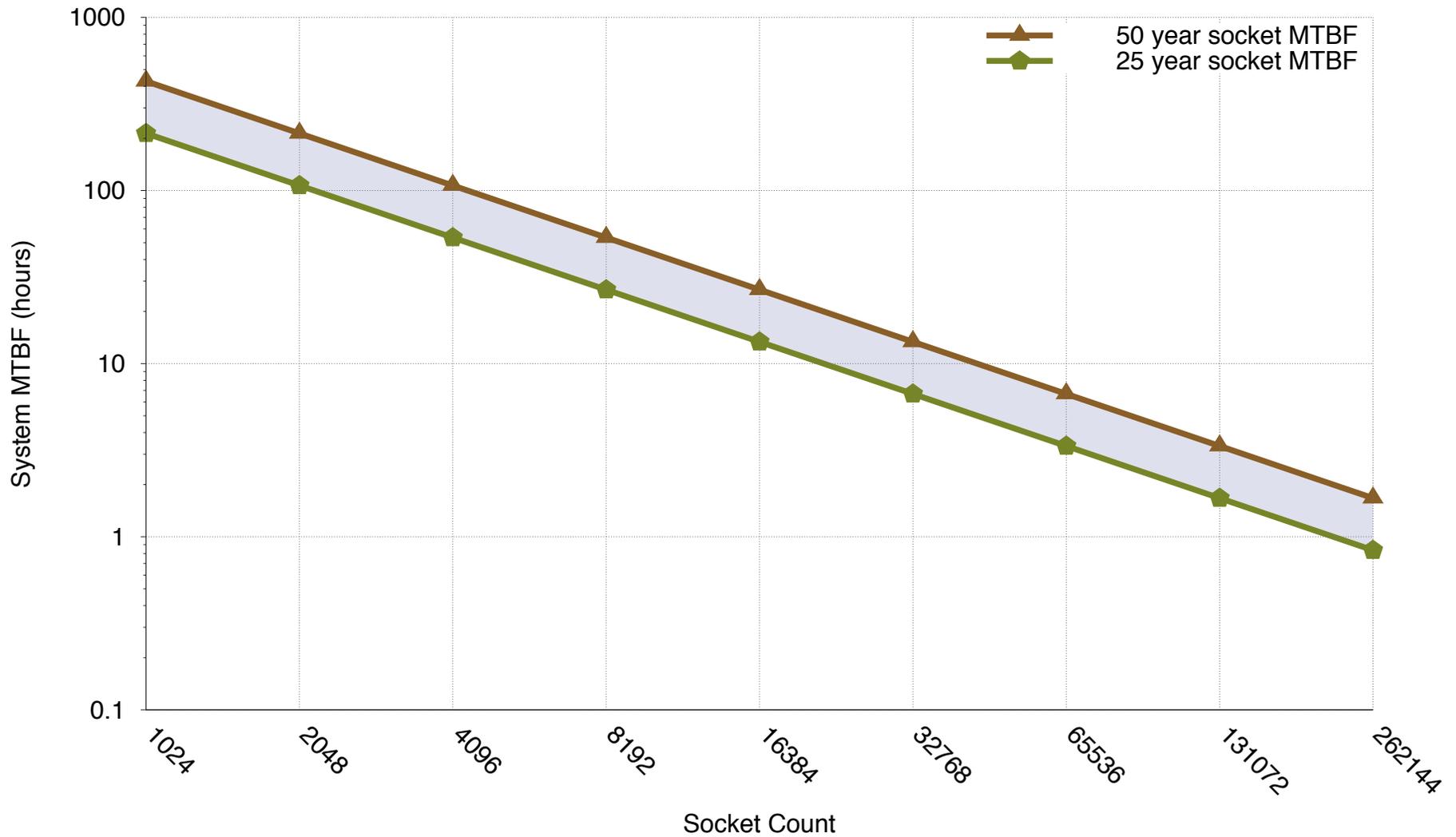


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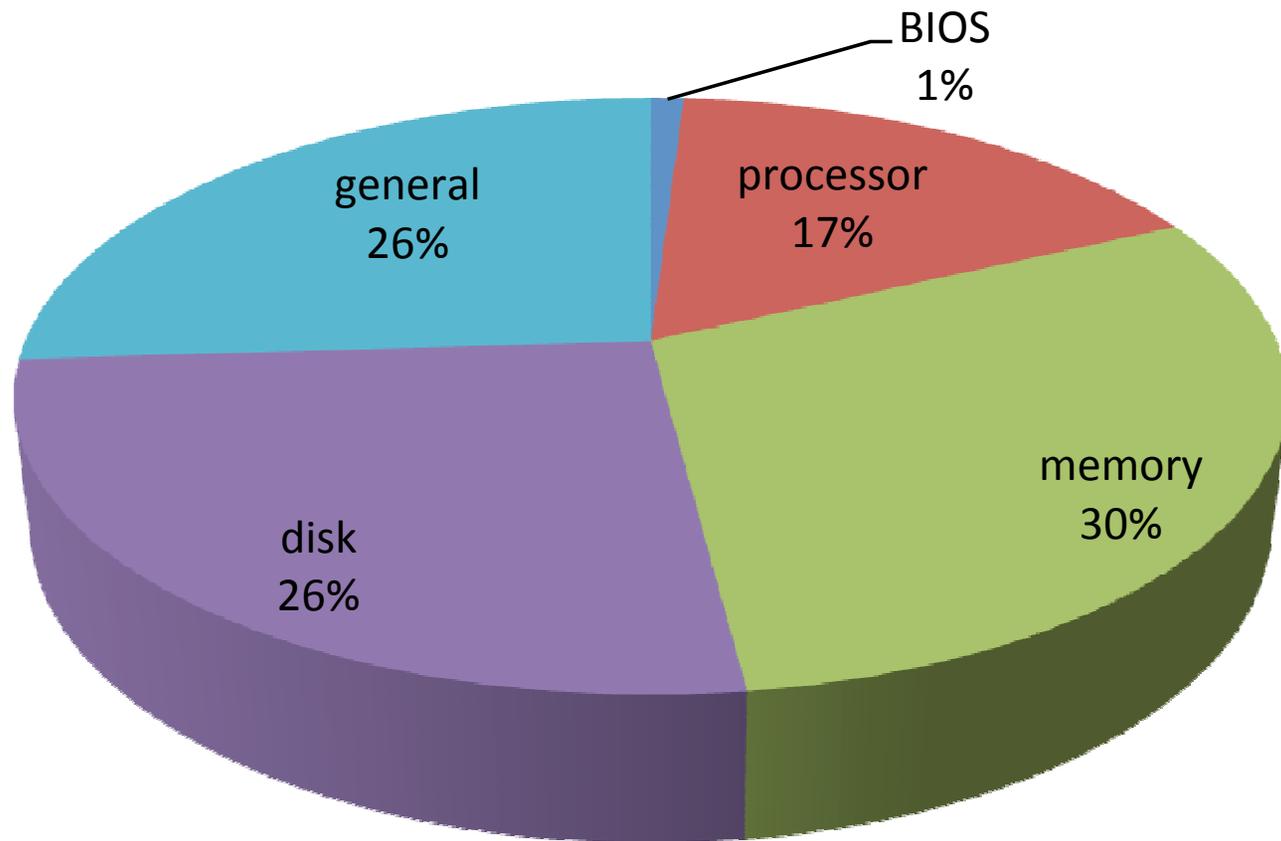
The Fastest Machines Are Getting Larger



... And Failures Are Becoming More Common

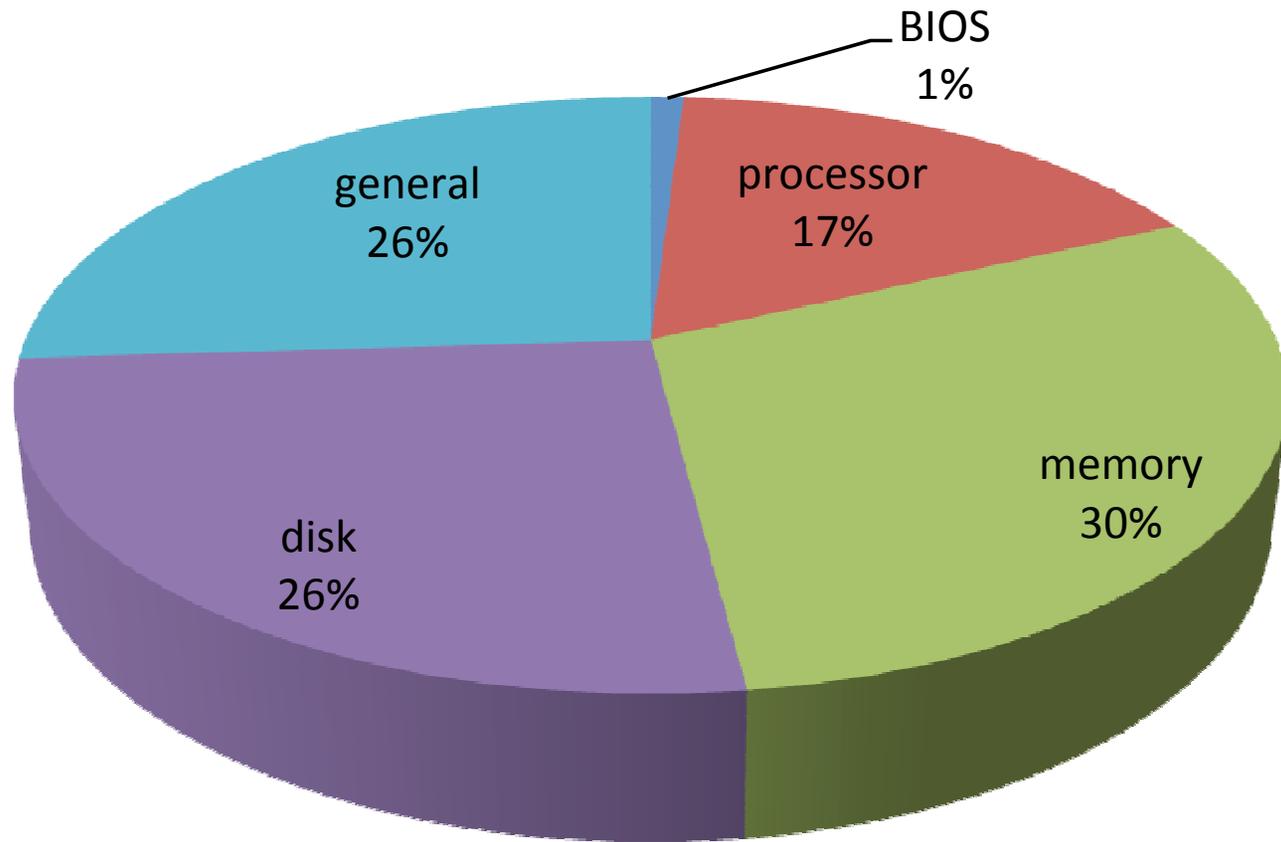


Most Common Hardware Failure Due to Memory



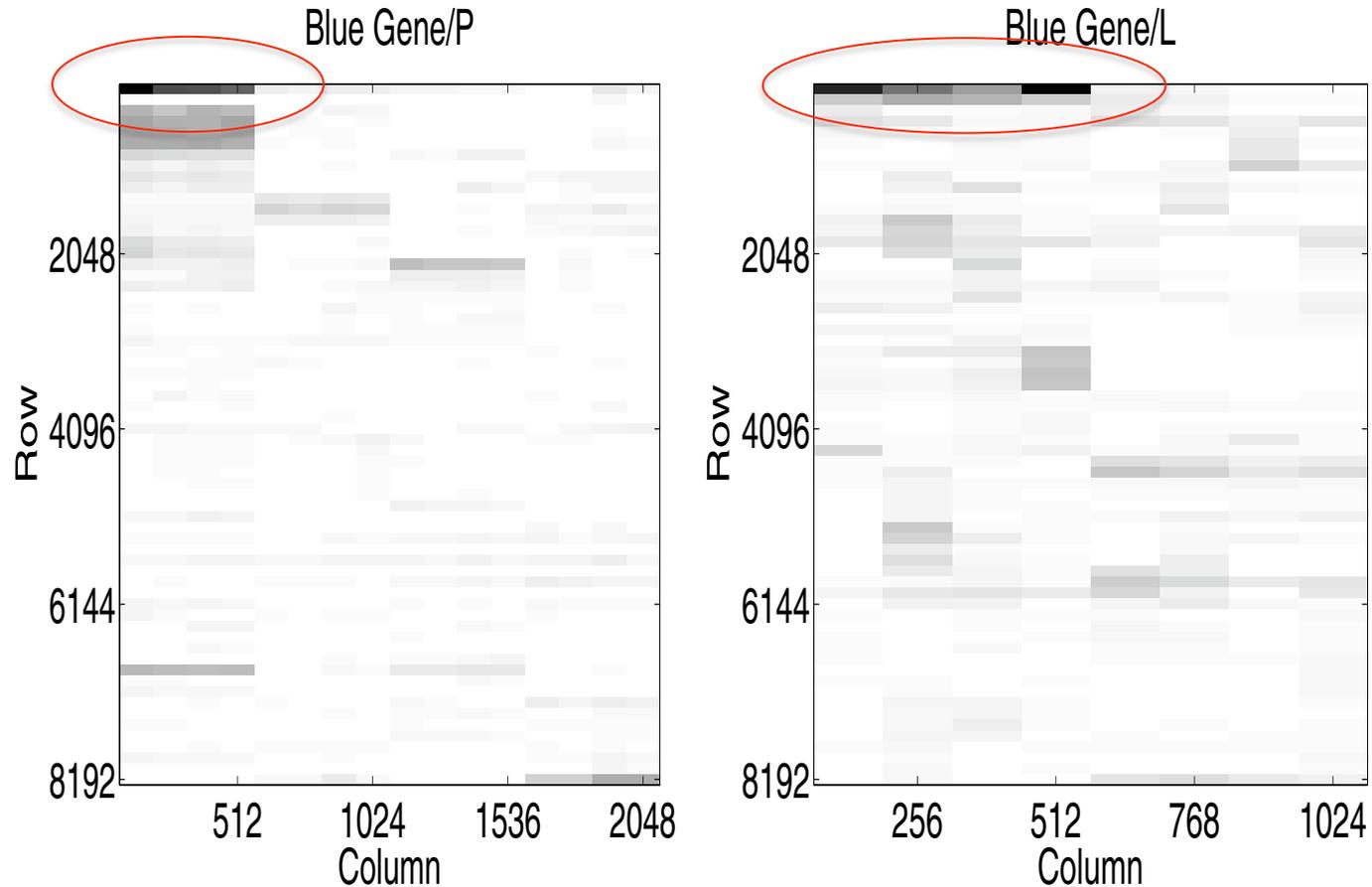
From "Automating Software Failure Reporting" by B. Murphy, *ACM Queue* 2, 2004

Most Common Hardware Failure Due to Memory



Memory failures expected to increase in future systems

Errors in OS Memory Shown To Be More Likely



From “Cosmic Rays Don’t Strike Twice: Understanding the Nature of DRAM Errors And the Implications for System Design” by A. Hwang et al, from *ASPLOS’12*

Current OS Handling of DRAM Failures

- Current OSs hard reboot for DRAM failures in OS memory

- If we can correct this error, we can avoid a restart and make forward progress

Our Goal

Construct an operating system/runtime resilient to soft errors.

- The resilient OS/runtime key to the scalability of extreme-scale systems
- A hardened OS/runtime can continue in the presence of failures
- A resilient OS and runtime critical to the emerging forward-error recovery methods
- These forward-error recovery methods are predicted to have lower overheads and avoid the wasted computation of current rollback/recovery methods

DRAM Failures: A Quick Refresher

- DRAM becoming largest portion of machines power budget
- Prevalence of errors in HPC due to number of DRAM modules (10K – 100K in current systems)
- Susceptibility due to a combination of quantity and density
- Power optimizations, for example decreased supply voltages and increased density, will further increase error rates
- Types of errors: single-bit correctable, double-bit detectable, multi-bit undetectable errors
- Uncorrectable errors becoming increasing common – 8% of all DIMMS/year on current systems

Current State of the Practice

- Single-symbol Error Correction and Double-symbol Error Detection (SEC-DED) but at a cost of increased energy and reduced performance
- Similarly for Chipkill which tolerates an entire DRAM chip failure
- Errors result in a Machine Check Exception (MCE) which logs the error and kills the application which memory belongs to
- Failures that occur in the OS typically result in a hard-reboot
- Common resilience methods (i.e. rollback recovery) focus only on application and not the OS

Our Approach: Compare Vulnerability of Linux and Kitten LWK



- Comparing two OSs similar to ones likely seen on an exascale-class system; Kitten and CLE
- Purpose of this evaluation is to look at the ease of protecting each respective OS to DRAM failure
- This initial study looks at a number of factors:
 - Code complexity. Metric: Source Lines Of Code (SLOC) count
 - Memory footprint of the OS while running an HPC application (LAMMPS)
 - Identifying representative critical state that must be protected
- These factors used to suggest failure mitigation mechanism. For example, small, simple state may effectively protected with redundancy

Kitten: A Next Generation Lightweight Kernel



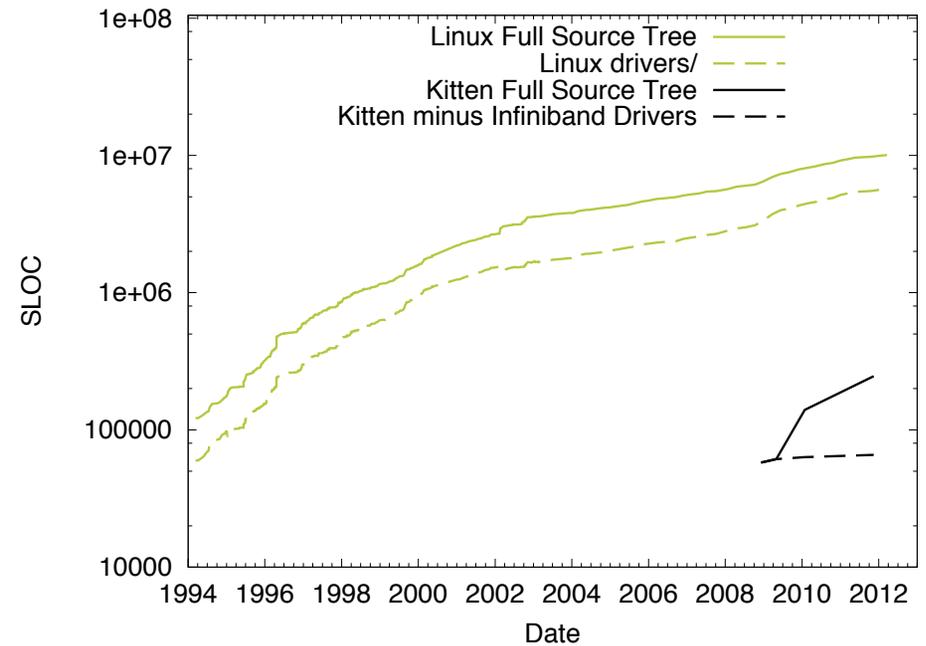
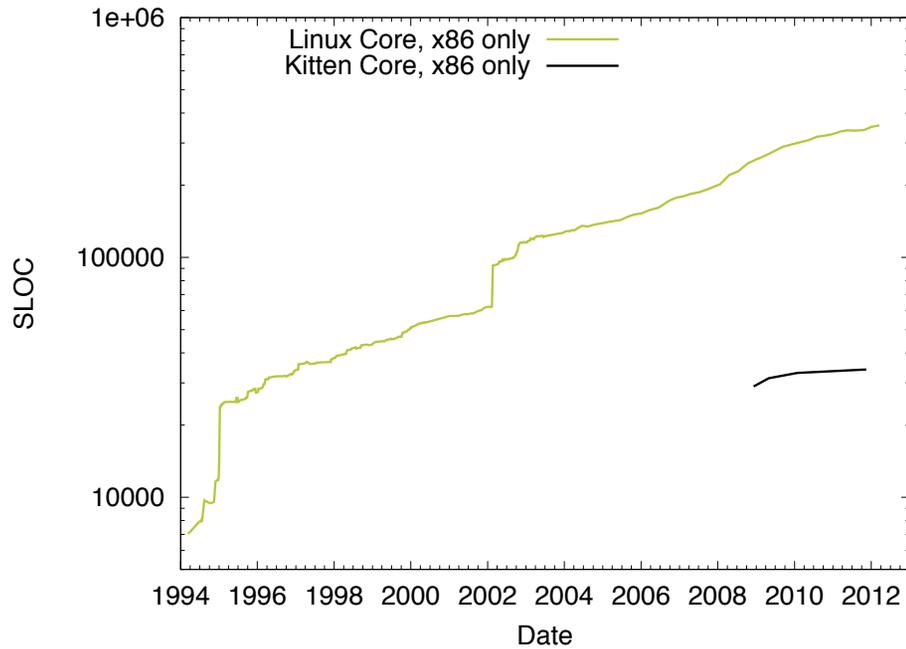
- A special-purpose, limited functionality OS developed at Sandia
- Latest in SUNMOS, Puma, Cougar, Catamount line of lightweight kernels
- Code base derived from Linux, therefore ABI compatible
- Compute node kernel providing only that functionality needed for a set of mission critical HPC applications
- Functionality not needed in kernel pushed into user space
- Full-featured guest OS can be loaded on-demand via the Palacios virtual machine monitor

Open Source: Kitten (<http://code.google.com/p/kitten>),
Palacios (<http://www.v3vee.org/palacios>)

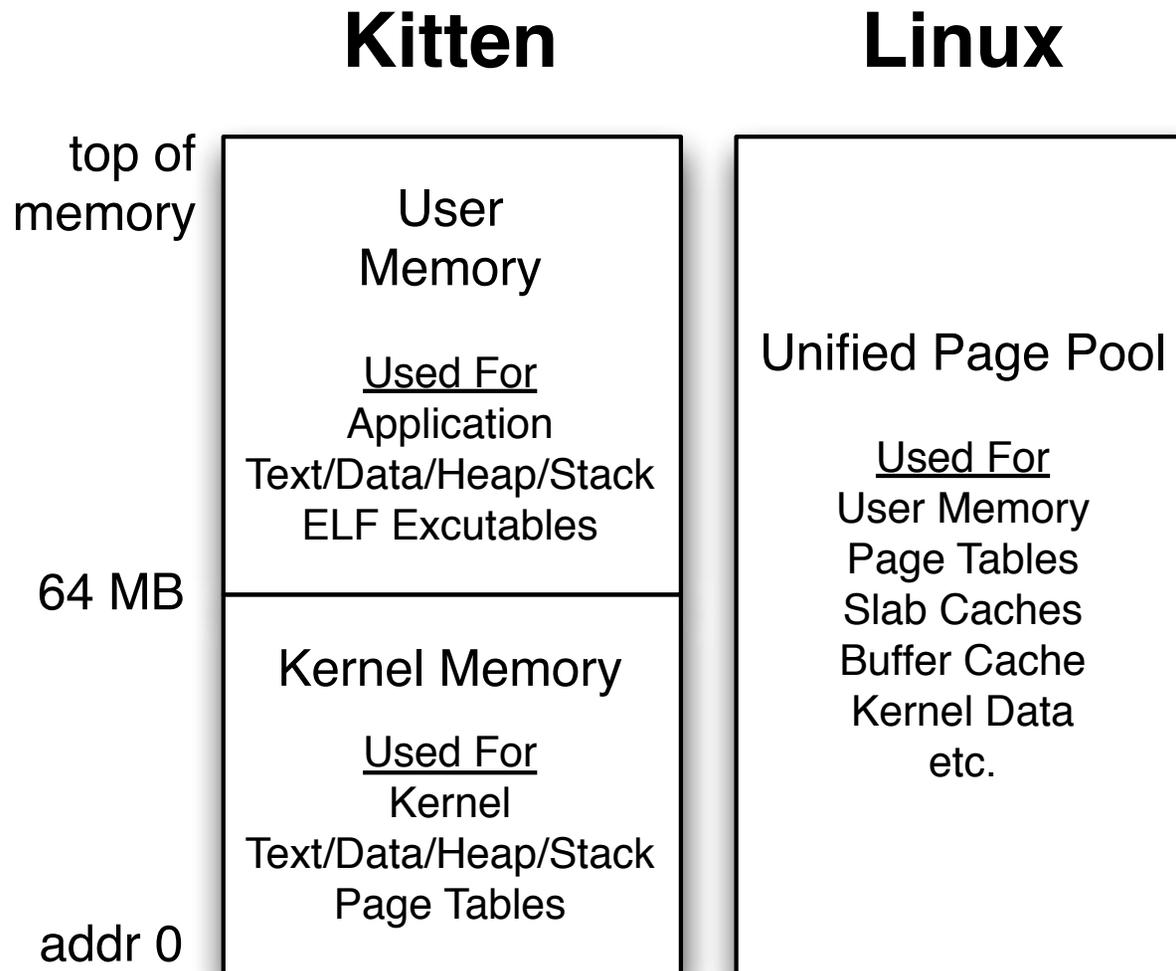
CLE: The Cray Linux Environment

- Cray's scalable OS for the XT and XE line of supercomputers
- Stripped-down kernels run on compute nodes while full featured kernels run on the IO nodes
- Both kernels based on the Linux general purpose OS
- Compute node optimizations include:
 - Enhancements to memory management
 - Improved out-of-memory handling
 - Modifications for decreased OS "jitter"
 - Forwarding of IO to full-featured nodes

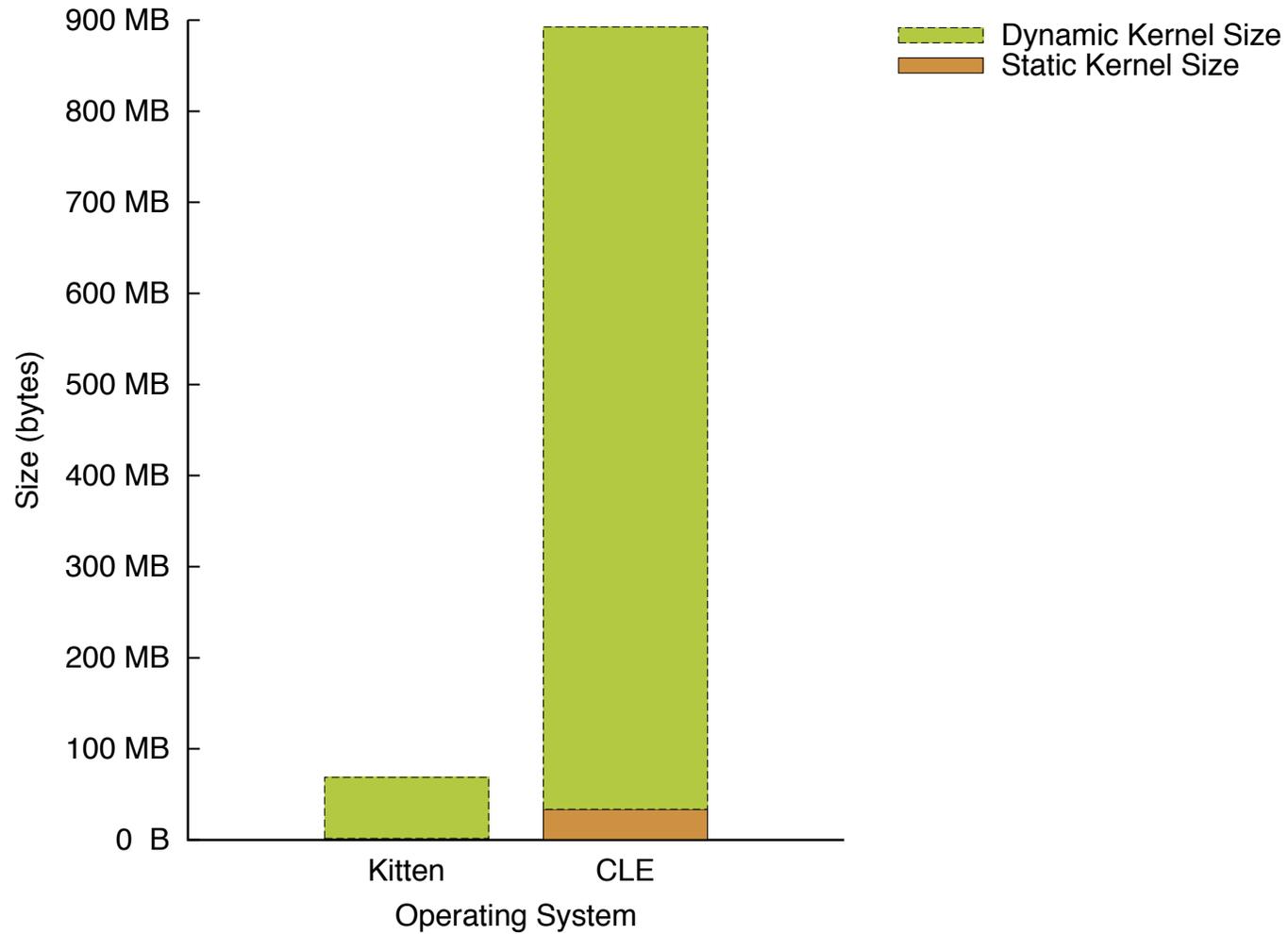
Kitten Significantly Less Complex Than CLE



Kitten Runtime Memory Footprint Bounded, Unlike Generic Linux



In Practice, CLE's Footprint is Also Bounded



Example of OS Critical State: Page Table Entries

- Correct PTEs critical to proper execution of an application
- Both Kitten and Linux store PTEs in kernel memory
- Memory used dependent on page size
 - 4K pages: 2MB per GB of application memory
 - 2MB pages: 8KB per GB of application memory
 - 1GB pages: 8B per GB of application memory
- Kitten always able to use larger page size due to its segment-based, static memory allocation policy
- Linux attempts to use larger page size but fragmentation is an issue
- Kitten's deterministic page mappings makes PTE verification as easy as storing a base and offset. Linux verification much more complicated
- Note: when a corrected PTE is found, computation must rollback as corrupted value may have been used

Summary

- DRAM failures in the OS a common error on current systems and expected to increase in frequency
- An OS resilient to these failures critical to scalability of extreme-scale systems
- In this work we focus on two HPC OSs likely seen on extreme-scale system: Kitten and Linux
- Presented the complexity of each OS in term of SLOC count, examine memory footprint, and evaluate vulnerability of critical state
- Overall, our results suggest hardening the Kitten LWK to be more tractable due to its smaller, deterministic state

Current and Ongoing Work

- Kitten our initial target for investigation due to its smaller, simpler, and largely static state
- Identification of critical state nearly complete
- Conducting analysis of failure mitigation methods, outlining both the space and performance overheads
- Where appropriate, mechanisms being evaluated for Linux
- Developed library to also allow applications to recovery from memory failures while avoiding rollback
- Errors in the OS beyond DRAM also being evaluated

Acknowledgements

9lives Resilience Group:

- Sandia
- UNM
- IBM
- NCSU
- ASU

**This work is supported by the Sandia National Laboratories
Laboratory Directed Research and Development (LDRD) program**

DOE Exascale OS/Runtime Technical Council

- Summarize the challenges of exascale OS/R
- Assess the impact on OS/R of exascale requirements of facilities and production support, applications and programming models, and hardware architectures
- Describe a model to interact with vendors such that there can be proprietary innovation but still support specific APIs that allow interoperability/portability and a minimum set of requirements for functionality
- Identify promising approaches to challenges and requirements by engaging the HPC research community and by drawing on novel approaches from other related areas such as embedded computing and cloud computing
- Articulate dependencies, conflicting requirements, and priorities of the OS/R research agenda
- Submit findings to the DOE Office of Science and NNSA in a report

10¹⁸ Call for Position Papers

Added by [Peter Beckman](#), last edited by [Peter Beckman](#) on Jun 19, 2012

PAPERS ARE DUE July 13, 2012

The PDF version of the Exascale Operating System and Runtime Software call for Position Papers:
[OSR_CallForPositionPapers.pdf](#)

Call for Position Papers: Operating System and Runtime Software for Exascale Systems

The research challenges associated with Exascale systems have been articulated in numerous reports. We clearly need new approaches to address these tremendous challenges. The Exascale Operating Systems and Runtime (OS/R) Technical Council (TC) has been convened by the Department of Energy (DOE) Office of Science and National Nuclear Security Administration to develop a research agenda and plan to address them. This activity will result in a report describing the research priorities and the process used to develop this plan. The report will be published in November 2012. As part of the process, we solicit community input, in the form of position papers that describe novel research approaches for exascale OS/R. Responsive submissions will be made public via the OS/R TC website and portions may be included in the final report. The OS/R TC will review these position papers and invite selected contributors to participate in a workshop to be held on October 4-5, 2012 in Washington, DC.

Necessary background information, including previous exascale reports and submission instructions, can be found on the public web pages for the OS/R TC: <https://collab.mcs.anl.gov/display/exaosr>

Requirements:

Position papers should describe a fundamental computer science research approach in the development of operating systems or runtime software to addresses the key challenges associated with exascale computing systems. This description should be followed by a brief summary of related work and an assessment of the approach based on the following dimensions:

- **Challenges addressed:** Which exascale OS/R challenges does this approach address?
- **Maturity:** What are the indicators that this approach will address the identified challenges?
- **Uniqueness:** To what extent is the proposed approach unique to Exascale systems? Could it be addressed by other research programs?
- **Novelty:** How is this approach different than existing solutions?
- **Applicability:** To what extent will the proposed approach, if successful, be applicable to other areas?
- **Effort:** How much effort is needed to effectively explore this approach?

Each position paper must be no more than two pages. The paper may include any number of authors, but must provide contact information for a single "contact" author. There is no limit to the number of position papers that an individual or group can submit. Authors are strongly encouraged to follow the structure presented above.